IHV-486/5x86 Single Board Computer User's Manual

For MCSI PART NO. 88000 IHV-486/5x86
All-In-One Single Board Computers
For Industrial/Embedded Systems Applications

MICRO COMPUTER SPECIALISTS, INC.
"The Embedded PC Specialists"
2598 Fortune Way
Vista, CA 92083
U.S.A.

Voice (760) 598-2177 - Fax (760) 598-2450
Technical Support BBS (760) 598-2179

Revised April 6, 1999
Revision 1.5

Changes are made periodically to the information contained herein; these changes will be incorporated into new editions of this document.

Requests for copies of this publication or the product(s) which it describes should be made to MCSI.

While every effort has been made to insure that this document and its accompanying product(s) are free from defects, MCSI, its distributors, representatives, and employees shall not be responsible for any loss of profit or any other commercial damage including, but not limited to, special, incidental, consequential, or other damages occasioned by the use of this product(s).

In the event of defect the buyer's sole recourse is to receive a refund or replacement unit at MCSI's discretion if notified within the time period covered by the product warranty.

PREFACE

This manual provides information about the MCSI IHV-486/5x86 All-In-One Single Board Computer. This information is intended for users who must implement IBM PC/AT compatible computer solutions to a wide variety of applications which cannot be satisfied using conventional desktop computers. This manual assumes that the reader has a good understanding of MS-DOS and the standard IBM PC/AT compatible architecture. For more information on the IBM PC compatible hardware and software architecture, refer to any of the many books available on the subject. A few suggestions are listed below:

- *Advanced MS-DOS Programming*, Microsoft Press
- *Programmers Guide to the IBM PC*, Microsoft Press
- *Programming the 80386*, Sybex
- *Undocumented DOS*, Addison Wesley

INVENTORY CHECKLIST

The complete IHV-486/5x86 All-In-One Single Board Computer package consists of the following:

IHV-486/5x86 All-In-One Single Board Computer
3½ Diskette containing VGA Video Drivers
PROMDISK-Chip Software Utilities with ROM-DOS ver 6.22 (optional)
This Manual

If any of the above is missing or appears to be damaged, inform MCSI immediately.

Table of Contents

SECTION 1 - INTRODUCTION

The IHV-486/5x86 All-In-One Single Board Computer (SBC) is a high performance system board that provides the primary elements for building an IBM PC/AT compatible computer for a wide variety of embedded systems applications. The IHV-486/5x86 SBC contains all the basic elements found in a standard IBM PC/AT compatible desktop computer system, plus some unique features which make it ideally suited for industrial applications. The most outstanding features include: an on-board SVGA display controller, a WatchDog timer, an optional PROMDISK-Chip™ Disk Emulator, single +5VDC operation, and a compact half size form factor. The optional PROMDISK disk emulator comes complete with the ROM-DOS version 6.22 operating system, and emulates a bootable hard disk drive with capacities up to 32M-bytes. The WatchDog timer and PROMDISK-Chip makes the board ideally suited for controlling critical processes where unattended operation is essential. The compact half size form factor makes it ideally suited for embedded applications.

The IHV-486/5x86 SBC is fully compatible with the IBM PC/AT (ISA Bus) which means virtually all the software written for the IBM PC/AT will run on the IHV-486/5x86 SBC.

FEATURES

A complete list of features is listed below:

- IBM PC/AT Compatible Plug-in Computer
- Supports 3.3V/3.45V 486/5x86/DX2/DX4 and AMD/Cyrix Microprocessors to 133Mhz
- Super VGA PCI Local Bus Video Controller with 1M-byte Video Memory
- ALI Chip Set
- AWARD BIOS
- Optional PROMDISK-Chip Disk Emulator includes ROM-DOS 6.22 Operating System
- Passive Backplane Architecture
- 64M-Byte Standard or EDO DRAM System Memory (2-72pin SIMMs)
- 128K High Speed Secondary Cache Memory
- PS2/AT Compatible Keyboard Port
- PS2 Compatible Mouse Port
- Two High Speed 16C550 Compatible RS-232 Serial Ports with ±15KV ESD Protection
- Multimode Bi-directional Parallel Printer Port
- Clock/Calendar with Battery Back-up
- Low Power CMOS Design
- Half Size AT Plug-in Multilayer Board for Low EMI and High Reliability
- WatchDog Timer and Power Monitor
- Dual Floppy Disk Port Supports Two 3.5" or 5.25" Drives up to 2.88M-bytes
- PCI Extended IDE Hard Disk Port
- On-board Mini Speaker
- Optional External Reset

SECTION 2 - SYSTEM DESCRIPTION

The following sections describe the major system features of the IHV-486/5x86 All-In-One Single Board Computer.

PROCESSOR

The IHV-486/5x86 SBC supports high performance low voltage (3.3/3.45V) 486/5x86/DX2/DX4 microprocessors from 25MHz to 100mhz, and up to 133MHz AMD/Cyrix 5x86 microprocessors. The 486/5x86 microprocessor includes an on-chip 8K-byte unified instruction cache, an 8K-byte data cache, an internal high performance math co-processor, and an enhanced 64-bit data bus. The on-board jumper selectable clock generator makes upgrading to a higher performance CPU easy. Some of the distinctive features of the processors include:

- 64-bit External Data Bus
- 32-bit Internal Architecture
- 128M-byte Directly Addressable Memory Space
- Internal 14 Word by 32-bit Register Set
- Separate 8K-byte Data and Cache Memories
- On-chip Pipelined Floating Point Processor
- Integrated Memory Manager

SYSTEM MEMORY (DRAM)

The IHV-486/5x86 SBC can support up to 64M-bytes of dynamic random access memory (DRAM) organized as two banks of 8Mx72 including eight parity bits. The board will support either standard or high performance EDO DRAM. The memory is configured using two single in-line memory module sockets, which will accept 72-pin single in-line memory modules (SIMMs) organized as 1MB, 2MB, 4MB, 8MB, 16MB, or 32MB with a maximum access time of 70ns. The following table demonstrates some of the most common memory configurations.

Typical Memory Configurations

Total Memory	Bank 0	Bank 1
1M	256Kx36	
2M	256Kx36	256Kx36
4M	1Mx36	
4M	512Kx36	512Kx36
8M	1Mx36	1Mx36
16M	4Mx36	
16M	2Mx36	2Mx36
32M	8Mx36	
32M	4Mx36	4Mx36
64M	8Mx36	8Mx36

Bank 0 = SIMM 1 Bank 2= SIMM 2
Note: SIMMs may be installed in either Bank first

CACHE MEMORY

The IHV-486/5x86 SBC includes 128K-bytes of cache memory for high speed access to blocks of data most recently read from main memory, including buffered data from the disk and video memory. The cache memory will significantly increase system performance over that of a conventional non-cached system.

DMA CONTROLLER

The IHV-486/5x86 SBC memory refresh and DMA functions are included in the System Controller chip which includes the equivalence of two 82C37 DMA controllers. The two DMA controllers are cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection for the two DMA devices thereby maintaining IBM PC/AT compatibility. The DMA channel assignments are listed below:

DMA Channel 0: Not Used (8-bit)
DMA Channel 1: Alternate for Multi-mode Parallel Port (8-bit)
DMA Channel 2: Floppy Disk (8-bit)
DMA Channel 3: Multi-mode Parallel Port (8-bit)
DMA Channel 5: Not Used (16-bit)
DMA Channel 6: Not Used (16-bit)
DMA Channel 7: Not Used (16-bit)

The DMA request (DRQx) and acknowledge (DACKx/) lines are available on the P1 98-pin edge connector.

INTERRUPT CONTROLLER

The IHV-486/5x86 SBC has the equivalence of two 82C59A interrupt controllers included in the System Controller chip. The controllers accept requests from peripherals, resolve priorities on pending interrupts and interrupts in service, interrupt the CPU, and provide the vector address of the interrupt service routine. The two interrupt controllers are cascaded in a fashion compatible with the IBM PC/AT. The interrupt priority and assignments are shown below in descending order of priority:

Highest	IOCHCK/	Parity Check (Non-maskable)
	IRQ0	System Timer (Not Available)
	IRQ1	Keyboard (Not Available)
	IRQ8	Real Time Clock (Not Available)
	IRQ9	SVGA Controller
	IRQ10	Not Used
	IRQ11	Alternate for Serial Port 2
	IRQ12	Alternate for Serial Port 1
	IRQ13	Co-processor (Not Available)
	IRQ14	Not Used
	IRQ15	Not Used
	IRQ3	Serial Port 2
	IRQ4	Serial Port 1
	IRQ5	Alternate for Parallel Port
	IRQ6	Floppy Disk Controller
Lowest	IRQ7	Parallel Port

The interrupt request lines IRQx and IOCHCK/ are available on the 98-pin edge connector except as noted on the previous page.

TIMERS

The IHV-486/5x86 SBC has the equivalence of an 82C54 Programmable Timer included in the System Controller chip. The 82C54 is a three channel Programmable Counter/Timer chip. The three timers are driven by a 1.19MHz clock source derived from the on-board 14.31818MHz crystal oscillator. The three timers are used as follows:

TIMER Channel 0: System Timer
TIMER Channel 1: Timer for DRAM refresh
TIMER Channel 2: Tone Generation for Audio

CLOCK/CALENDAR AND CMOS RAM

The IHV-486/5x86 SBC uses a Dallas DS12887 which is the equivalence of an MC146818 real time clock/calendar with 128 bytes of CMOS RAM. An internal lithium battery provides power to the RTC chip for at least ten years when the system power is off.

The 128 byte CMOS RAM consists of 14 bytes used by the clock/calendar, and 114 bytes used by the system BIOS.

Should your CMOS become corrupted, i.e. loss of battery power or accidentally clobbered, strange errors may occur while attempting to run your programs. Refer to Section 3.0 for instructions on resetting the initial SETUP values.

KEYBOARD PORT

The IHV-486/5x86 SBC contains an IBM PC/AT compatible keyboard controller for interfacing to a generic IBM PC/AT compatible keyboard. The keyboard controller assembles the serial data from the keyboard into bytes and interrupts the CPU via IRQ1 after each byte is ready to be read. The IRQ1 service routine reads port 60H to get the keyboard scan code and acknowledges by sending a positive pulse to port 61H to clear the interrupt for the next byte. Refer to Appendix D for the keyboard connector location and pin assignments.

MOUSE PORT

The IHV-486/5x86 SBC contains an IBM PS2 compatible mouse port for interfacing to a generic serial mouse. The mouse port controller assembles the serial data from the mouse into bytes and interrupts the CPU via IRQ1 after each byte is ready to be read. The IRQ1 service routine reads port 60H to get the scan code and acknowledges by sending a positive pulse to port 61H to clear the interrupt for the next byte. Refer to Appendix D for the mouse port connector location and pin assignments.

SPEAKER PORT

The IHV-486/5x86 SBC contains an on-board sub-miniature audio speaker to provide audio interface to the user. Because of the small size of the speaker, the sound output is much reduced over that of the larger speaker found in most desktop computers. A connector is provided to connect an external

speaker if the sound output is not sufficient. Refer to Appendix D for the speaker port connector location and pin assignments.

RESET SWITCH

The IHV-486/5x86 SBC includes an on-board power detector and power on reset circuit to reset the computer after power is applied, and to hold the computer reset during low power, brown-out conditions. In addition, there are provisions for connecting an external, normally open, push button reset switch. Refer to Appendix D for the reset switch connector location and pin assignments.

PRINTER PORT

The IHV-486/5x86 SBC contains a multimode parallel port which has the equivalence of an IBM PC/AT Parallel Printer Port. The multimode parallel printer port supports the PS/2 type bi-directional parallel port (SPP), the enhanced parallel port (EPP), and the extended capabilities port (ECP) parallel port modes. The port can be configured as a standard IBM PC/AT compatible LPT1, LPT2, or LPT3 printer port, or disabled completely using the CMOS Setup utility. Refer to Appendix D for the connector location and pin assignments.

SERIAL PORTS

The IHV-486/5x86 SBC has the equivalence of two NC16C550 UARTs. The two UARTs can be configured as standard IBM PC/AT RS-232C compatible COM1, COM2, COM3, or COM4 serial ports or individually disabled using the CMOS Setup utility. The serial ports use an enhanced RS-232 interface chip which provides ±15KV ESD protection. The data rates are independently programmable up to 115.2K baud. Refer to Appendix D for the connector location and pin assignments.

FLOPPY DISK PORT

The IHV-486/5x86 SBC contains an IBM PC/AT compatible dual floppy disk port with the equivalence of an NEC PD72056B Floppy Disk Controller, an on-chip digital data separator, and an IBM PC/AT compatible floppy disk adapter bus interface circuit. The Floppy Disk Port can be disabled by using the CMOS Setup utility. An on-chip digital data separator provides optimum performance with the following disk drive types:

5.25"	360K Double-Sided
3.5"	720K High Capacity
5.25"	1.2M High Capacity
3.5"	1.44M High Density
3.5"	2.88M High Density

Refer to Appendix D for the connector location and pin assignments.

ENHANCED IDE HARD DISK PORT

The IHV-486/5x86 SBC contains a PCI Extended Integrated Drive Electronics (IDE) Port which directly interfaces to two hard disk drives with embedded controllers. The IDE Disk Port can be disabled using the CMOS Setup utility. Refer to Appendix D for the connector location and pin assignments.

OPTIONAL PROMDISK-CHIP DISK EMULATOR

The IHV-486/5x86 includes a 32-pin socket designed to accept the MCSI PROMDISK-Chip. The PROMDISK-Chip Disk Emulator is a unique Flash Memory array which emulates a bootable read/write hard disk drive. The PROMDISK-Chip is offered in 4M, 8M, 16, and 32M byte capacities and comes complete with ROM-DOS version 6.22 installed. The PROMDISK-Chip occupies a 32K block of memory space above 640K, whose starting address is selected by jumper JP20. The PROMDISK-Chip uses the Datalight CardTrick® VBF integrated Flash File System and boot utilities.

The CardTrick Variable Block Flash (VBF) File System and ROM-DOS allow the PROMDISK-Chip to operate as a non-volatile Read/Write disk drive. This means that you can list directories, copy files, and read and write the Flash memory on PROMDISK-Chip through standard DOS interrupts and commands.

SVGA DISPLAY PORT

The IHV-486/5x86 SBC includes a Cirrus Logic CL-GD54M40 Super VGA graphic accelerator and display controller which interfaces directly to the local on-board PCI bus. The SVGA display port is fully compatible with IBM VGA, EGA, CGA, and MDA display adapters, and provides improved performance and additional functionality. The board includes 1M-bytes of high speed video SRAM. The SVGA display controller supports the following display resolutions:

1024x768 256 Colors (1M VRAM)
1280x1024 16 Colors (1M VRAM)

WATCHDOG TIMER

The IHV-486/5x86 SBC includes a WatchDog Timer circuit. The WatchDog Timer ensures that if an application program gets "lost or bombs", the system will reset or a non-maskable interrupt will be issued to the CPU. The WatchDog Timer is enabled by reading I/O port 443H. Once enabled, the WatchDog Timer must be triggered by reading I/O port 443H within the time out period, otherwise the WatchDog Timer will force a hardware reset or activate the IOCHCK/ line, generating a non-maskable interrupt (NMI). The WatchDog Timer can be disabled by reading I/O port 43H. A jumper is provided to select the time out period and to enable the WatchDog Timer circuit. Refer to Appendix E for the WatchDog Timer configuration jumpers.

SECTION 3 - SETUP

The IHV-486/5x86 SBC uses the latest AWARD BIOS which contains an internal Setup Utility for configuring the system. The system configuration settings are stored in the on-board CMOS memory which is backed up by a Lithium battery. Should your CMOS become corrupted, i.e. loss of battery power or accidentally clobbered, strange errors may occur while attempting to run your programs. If this occurs select the LOAD BIOS DEFAULTS from the MAIN SETUP MENU or use the **Del** key.

The Setup Utility can be invoked by first causing a cold boot (reset) or a warm boot (**Cntrl Alt Del)** and pressing the **Del** key when instructed. This will cause the memory diagnostics to be aborted and the Setup Utility to display the MAIN SETUP MENU. Using the →↑↓← cursor keys, move the highlighted bar to the option you wish to modify and then press **Enter** to select it. When in the MAIN SETUP MENU, the **F2** key is used to select the colors used in the setup screens, and the **F10** key is used to save the changes before exiting the Setup Utility. The **Esc** key may be used to exit the Setup Utility without saving the changes. The **PgUp** and **PgDn** keys are used to scroll through the selections for a given setting. **PgUp** is also used to increase the setting and **PgDn** to decrease the setting. In addition, you may also enter the setup utility directly by pressing the **Cntrl Alt Esc** simultaneously.

After making the desired selections from the various setup menus, you can save your selections by pressing the **F10** key or by selecting the appropriate selection from the MAIN SETUP MENU.

Notes:

1. The user should be aware that improper selection of certain values in the BIOS FEATURES SETUP UTILITY may cause unpredictable results. If this occurs select the MAIN SETUP MENU and then select the LOAD BIOS DEFAULTS to load the BIOS default values.

SECTION 4 - USING THE PROMDISK-CHIP DISK EMULATOR

The PROMDISK-Chip Disk Emulator operates as a Read/Write fixed disk drive. The paragraphs that follow describe how to use the optional PROMDISK-Chip.

USING ROM-DOS AND OTHER DISK OPERATING SYSTEMS

The PROMDISK-Chip has been pre-configured at the factory with the latest version of the Datalight ROM-DOS disk operating system. In addition, a current copy of the operating system is supplied on a floppy diskette.

If the operating system is accidentally erased from the PROMDISK-Chip it may be restored using the SYS command. The DOS format utility should not be used to restore the operating system.

To change the operating system version or type you should simply use the equivalent DOS SYS command to transfer the operating system.

PROMDISK LOW LEVEL FORMAT

The Flash memory contained on the PROMDISK-Chip board was initialized with the Datalight CardTrick low level format at the factory. During normal operation the Flash memory should never require reformatting unless there is a serious hardware or software malfunction. In the event it has been determined that the low-level format is corrupted, proceed as follows:

1. At the DOS prompt, run the PROMDISK-Chip low-level format utility PDCFMT.EXE located on the distribution diskette in the PDCHIP subdirectory.
2. Install a bootable floppy diskette in drive A and boot the system.
3. At the DOS prompt type SYS C: to transfer a bootable copy of DOS to PROMDISK-Chip.
4. Remove the floppy diskette from drive A: and reboot the system from PROMDISK-Chip.

CAUTION: Do Not use the DOS Fdisk utilities on the PROMDISK-Chip.

SECTION 5 - INSTALLATION

This section describes the procedures for installing the IHV-486/5x86 All-In-One Single Board Computer into your system. The following is a list of typical peripherals required to build a minimum system:

- Passive Backplane and Power Supply
- IBM PC/AT Type Keyboard
- Display Monitor
- Floppy or Hard Disk with MS-DOS, ROM-DOS, or PROMDISK Disk Emulator

INSTALLING THE SIMMS

When installing or removing the DRAM SIMMs, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the SIMMs:

1. Insert the first SIMM edge connector at a slight angle into either the SIMM1 or SIMM2 socket. Note that the SIMMs are keyed and will only go in one way.

2. Push the SIMM back into the connector carefully until it snaps into place.

3. Check to make sure the SIMM is inserted securely.

4. If required insert the second SIMM edge connector at a slight angle into the remaining SIMM socket.

To remove a SIMM, use a small screw driver to pull back the holding clip on each side of the SIMM and lift the SIMM from the connector.

INSTALLING THE CPU

When installing or removing the CPU, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the CPU:

1. Align pin one (white dot or beveled edge) on the CPU chip with pin one of the of the CPU socket. Note pin 1 of the CPU socket is located on the top left corner. To complete the installation gently press the CPU chip into place.

2. Double check the insertion and orientation of the chip before applying power. Improper installation will result in permanent damage to the chip.

To remove the CPU chip, insert a small screwdriver between the CPU and the socket and gently pry around the edge until the CPU is released from the socket.

INSTALLING THE PROMDISK-CHIP

When installing or removing the PROMDISK-Chip, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the PROMDISK-Chip:

1. Align pin one (white dot) on the PROMDISK-Chip with pin one of socket U7 on the CPU board.

2. Push the PROMDISK-Chip into the socket carefully until it is fully seated.

3. Check to make sure the PROMDISK-Chip is installed securely, and there are no bent pins.

To remove the PROMDISK-Chip, insert a small screwdriver between the PROMDISK-Chip and the socket and gently pry around the edge until the PROMDISK-Chip is released from the socket.

COMPLETING THE INSTALLATION

To complete the installation, the following steps should be followed:

1. Set the configuration jumpers in accordance with Appendix E.

2. Install the IHV-486/5x86 SBC into one of the I/O slots in a passive backplane.

3. Connect the applicable I/O cables and peripherals, i.e. floppy disk, IDE hard disk, monitor, keyboard, power supply, etc.

4. Connect an IBM PC compatible keyboard.

5. Turn power on to the display monitor.

6. Turn power on to the backplane power supply.

7. After the BIOS sign-on message is displayed, press the **Del** key to enter the Setup Utility.

8. Reconfigure the IHV-486/5x86 CMOS using the internal SETUP.

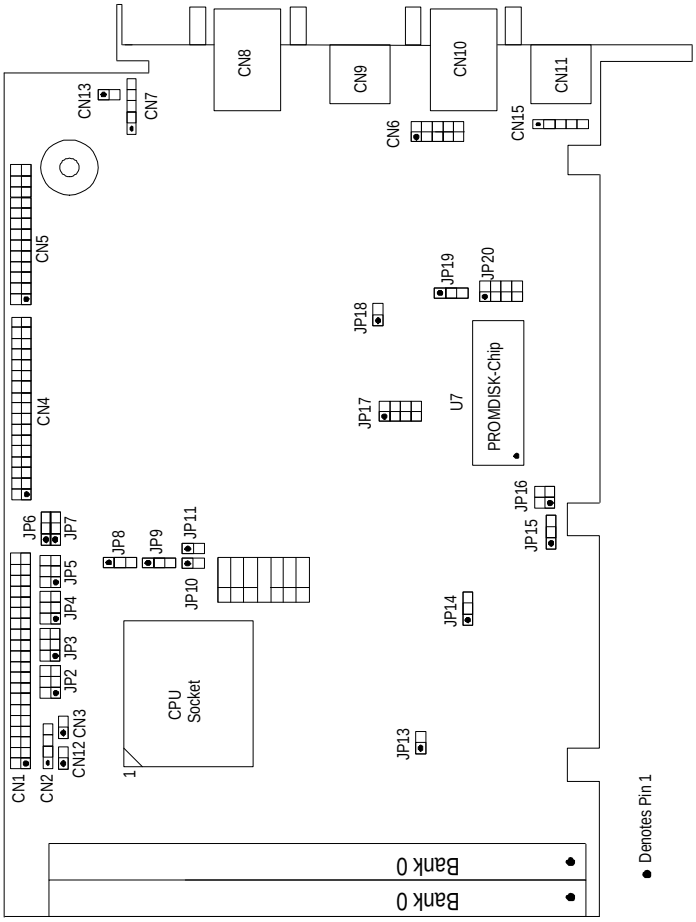
9. Boot the system.

APPENDIX A - SPECIFICATIONS

This appendix lists the specifications for the IHV-486/5x86 All-In-One Single Board Computer.

CPU:	Supports: 486/5x86/DX2/DX4 and AMD/Cyrix 5x86 3.3V/3.45V microprocessors, up to 133MHz.
Co-processor:	Internal to the 486/5x86 Chip
Memory:	System Memory Expandable to 64M-bytes. Supports 512Kx36, 1Mx36, 2Mx36, 4Mx36, or 8Mx36 SIMMs using two 72-pin SIMM sockets. Both standard and high performance EDO DRAM is supported. Internal 8K-byte Data and 8K-byte Instruction Cache Memory. 128K High Speed Cache Memory.
BIOS:	AWARD BIOS with Internal SETUP and ROM defaults
Clock/Cal:	PC/AT Compatible with internal Lithium battery back-up
I/O Bus:	IBM PC/AT Compatible 98-pin Edge Connector
DMA:	7 Channels (4 8-bit & 3 16-bit)
Timers:	3 Programmable
Interrupts:	16
Reset:	Controlled by on-board power detector with provisions for external reset switch at header CN12
I/O Ports:	2 - RS-232 Serial Ports COM1 at rear connector CN10, and COM2 at header CN6 1 - Parallel Printer Port at header CN5 1 - PS2 Keyboard Port at header CN7 and at rear PS2 type connector CN11 1 - On-board Speaker with Speaker Port at header CN2 1 - Dual 3.5"/5.25" Floppy Disk Port at header CN4 1 - Enhanced IDE Hard Disk Port at header CN1 1 - WatchDog Timer 1 - PS2 Mouse Port at rear connector CN9
PCI Video Port:	1 - PCI SVGA Video Port at rear connector CN8 Chipset: Cirrus Logic CL-GD54M40 VRAM: 1M-byte Resolution: 1024x768 256 Colors, 1280x1024 16 Colors
PROMDISK Port:	1- 32pin socket (U7) supports MCSI 4M, 8M, 16M, or 32M PROMDISK-Chip
Speed:	25-133MHz jumper selectable.
Battery:	Lithium for Clock/Calendar & CMOS RAM (ten years typical)
Benchmark:	LANDMARK v2.0 =444MHz for 133MHz AMD5x86 P75
Size:	Half Size AT board 7.1"L X 4.8"H
Weight:	12 Oz.
Power:	+5VDC @ 2.5A

APPENDIX B - BOARD OUTLINE



APPENDIX C - MEMORY AND I/O MAPS

The following is the memory map for the IHV-486/5x86 SBC. The addresses are fully PC/AT compatible, unless otherwise specified.

IHV-486/5x86 SBC Memory Map

Address	Used For	Size
00000H - 003FFH	Interrupt Vectors	1.0K
00400H - 005FFH	BIOS Values	0.5K
00600H - 9FFFFH	User RAM (DOS)	638.5K
A0000H - AFFFFH	Reserved for EGA*	64.0K
B0000H - B7FFFH	Video RAM (MDA)*	32.0K
B8000H - BFFFFH	Video RAM (CGA)*	32.0K
C0000H - C3FFFH	VGA BIOS	16.0K
C4000H - C7FFFH	EMS Window	16.0K
C8000H - CFFFFH	Reserved	32.0K
D0000H - E7FFFH	ROM Scan Devices*	96.0K
E0000H - EFFFFH	ROM Scan Devices*	64.0K
F0000H - FFFFFH	System BIOS	64.0K
100000H - 3FFFFFFH	User Memory	64.0M

External to the IHV-486/5x86

The following is the I/O map for the IHV-486/5x86 SBC. I/O addresses are fully PC/AT compatible, unless otherwise specified.

IHV-486/5x86 SBC I/O Map

Address	Function
000H - 01FH	DMA Controller #1
020H - 021H	Interrupt Controller #1
022H - 023H	Configuration Address Register
040H - 05FH	System Timers
060H - 063H	Keyboard, Status, & System Control
070H - 07FH	Clock/Calendar & CMOS Ram Access
080H - 083H	DMA Page Register
0A0H - 0BFH	Interrupt Controller #2
0C0H - 0DFH	DMA Controller #2
0F0H	Clear Math Co-processor Busy
0F1H	Reset Math Co-processor
1F0H - 1F8H	IDE Hard Disk
278H - 27FH	Parallel Printer Port LPT2
2E8H - 2EFH	Serial Port COM4
2F8H - 2FFH	Serial Port COM2
378H - 37FH	Parallel Printer Port LPT1
3BCH - 3BFH	Parallel Printer Port LPT3
3E8H - 3EFH	Serial Port COM3
3F0H - 3F7H	Floppy Disk Controller
3F8H - 3FFH	Serial Port COM1
443H	WatchDog Timer

APPENDIX D - CONNECTORS

CN7 Keyboard Header/Connector

Pin	Signal
1	KBCLK
2	KBDATA
3	N/C
4	GND
5	+5VDC

CN4 Floppy Disk Port Connector

Pin	Signal Name
2	RPMLC
4	Not Used
6	Not Used
8	INDEX/
10	MOTOR0/
12	DRIVE SELECT1/
14	DRIVE SELECT0/
16	MOTOR1/
18	DIRECTION
20	STEP/
22	WRITE DATA/
24	WRITE GATE/
26	TRACK0/
28	WRITE PROTECT/
30	READ DATA/
32	HEAD SELECT/
34	DISK CHANGE/

All odd numbered pins are GND

CN1 Enhanced IDE Hard Disk Port Connector

Pin	Signal	Pin	Signal
1	IDERST/	2	GND
3	IDED7	4	IDED8
5	IDED6	6	IDED9
7	IDED5	8	IDED10
9	IDED4	10	IDED11
11	IDED3	12	IDED12
13	IDED2	14	IDED13
15	IDED1	16	IDED14
17	IDED0	18	IDED15
19	GND	20	Not Used
21	Not Used	22	GND
23	IDEIOW/	24	GND
25	IDEIOR/	26	GND
27	Not Used	28	IDEALE
29	Not Used	30	GND
31	IRQ14	32	IOCS16/
33	IDESA1	34	Not Used
35	IDESA0	36	IDESA2
37	HDCS0/	38	HDCS1/
39	IDEACT/	40	GND

CN5 Printer Interface Connector

Pin	Signal	Pin	Signal
1	STROBE/	14	AUTOFD/
2	PDAT0	15	ERROR/
3	PDAT1	16	INIT/
4	PDAT2	17	SLCTIN/
5	PDAT3	18	GND
6	PDAT4	19	GND
7	PDAT5	20	GND
8	PDAT6	21	GND
9	PDAT7	22	GND
10	ACK/	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT	26	GND

CN10 Serial Port #1 9-pin Sub D Connector

Pin	Signal Name
1	CARRIER DETECT #1
2	RECEIVE DATA #1
3	TRANSMIT DATA #1
4	DATA TERMINAL READY #1
5	GND
6	DATA SET READY #1
7	REQUEST TO SEND #1
8	CLEAR TO SEND #1
9	RING INDICATOR #1

CN6 Serial Port #2 10-pin Header/Connector

Pin	Signal Name
1	CARRIER DETECT #2
2	DATA SET READY #2
3	RECEIVE DATA #2
4	REQUEST TO SEND #2
5	TRANSMIT DATA #2
6	CLEAR TO SEND #2
7	DATA TERMINAL READY #2
8	RING INDICATOR #2
9	GND
10	NOT USED

CN11 Keyboard Connector (PS2 type)

Pin	Signal
1	KBDATA
2	N/C
3	GND
4	+5VDC
5	KBCLOCK
6	N/C

CN12 Reset Header/Connector

Pin	Signal Name	Description

1	RESET/	Connect to switch, ground this pin to reset
2	GND	Ground

CN2 Speaker Port Header/Connector

Pin	Signal Name	Description
1	SPEAKER	Connect to Speaker (-)
2	N/C	
3	GND	Ground
4	+5VDC	Connect to Speaker (+)

CN3 IDE LED Header/Connector

Pin	Signal Name	Description
1	+5VDC	Connect to IDE LED anode (+)
2	IDE LED	Connect to IDE LED cathode (-)

CN9 PS2 Mouse Connector

Pin	Signal
1	MSDATA
2	N/C
3	GND
4	+5VDC
5	MSCLK
6	N/C

CN13 Auxiliary Power Connector

Pin	Signal Name
1	+5VDC
2	GND

CN15 Keylock Header/Connector

Pin	Signal Name	Description
1	LED POWER (+)	Connect to anode of power LED
2	N/C (Key)	N/C (Key)
3	GND	Connect to cathode of power LED
4	KBLOCK/	Connect to ground to inhibit keyboard
5	GND	Ground

APPENDIX E - CONFIGURATION JUMPERS

JP14 CPU Power Selection Jumper

CPU Voltage	JP14
3.3VDC	2-3
3.45VDC	1-2

JP2-10 CPU Selection Jumpers

CPU	JP2	JP3	JP4	JP5	JP6	JP7	JP8	JP9	JP10
Intel 486DX2/DX4 &E	OFF	3-4	3-4	3-4	2-3	2-3	1-2	OFF	ON
AMD 486DX4+ Cyrix 5x86 Intel 486DX2/DX4 &EW SGS ST486DX2V (3.3V) ST486DX4V (3.3V)	5-6	3-4	3-4	3-4	2-3	2-3	2-3	2-3	ON
Cyrix/TI/SGS DX2/DX4	1-2	5-6	5-6	5-6	2-3	2-3	1-2	1-2	ON
AMD 486DX/DX2/DX4	OFF	OFF	OFF	1-2	2-3	2-3	1-2	OFF	OFF
AMD 5x86-P75 (133) AMD DX2+ (SV8B)	1-3 5-6	3-4	3-4	3-4	2-3	2-3	2-3	2-3	ON

JP11 AMD DX4 (SV8B) Cache Control Jumper

OFF	Write Back Internal Cache
ON	Write Thru Internal Cache

JP13, JP15, & JP16 CPU Clock Speed Selection Jumpers

CPU Clock	JP13	JP15	JP16
25MHz	OFF	1-2	OFF
33MHz	OFF	1-2	1-2 3-4
40MHz	ON	2-3	3-4

Note: DX2/DX4-100 & 5x86-100 use 33MHz CPU Clock
DX2-80/DX4-120 & 5x86-120 use 40MHz CPU clock
AMD 5x86-133 use 33MHz CPU clock

JP18 PS/2 Mouse Enable Jumper

ON	Enabled, IRQ12 (Default)
OFF	Disabled

JP19 WatchDog Timer Control Jumper

1-2	Generates hardware RESET when time out occurs. (Default)
2-3	Generates NMI (IOCHRDY) when time out occurs.
OFF	Disable

JP17 WatchDog Timer Time-out Period Jumper

Time	1-2	3-4	5-6	7-8
1second	OFF	OFF	ON	OFF
2 seconds	OFF	OFF	ON	ON
10 (Default)	OFF	ON	OFF	OFF
20 seconds	OFF	ON	OFF	ON
110 seconds	ON	OFF	OFF	OFF
220 seconds	ON	OFF	OFF	ON

JP20 PROMDISK-Chip Address Selection Jumper

Address Segment	JP20
D000H	1-2
D800H	3-4
E000H	5-6
Special Do Not Use	7-8

APPENDIX F - BIOS ERROR BEEP CODES

During the POST (Power On Self Test) routines, which are performed each time the system is powered on, errors may occur.

Nonfatal errors are those which, in most cases, allow the system to continue the boot up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with MCSI Customer Service for possible repairs.

These fatal errors are communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of number eight, are fatal errors.

No. of Beeps	Error Message
1	**Refresh Failure** - The memory refresh circuitry is faulty.
2	**Parity Error** - A parity error was detected in the first 64K block of system memory.
3	**Base 64KB Memory Failure** - A memory failure occurred within the first 64KB of memory.
4	**Timer Not Operational** - Timer #1 has failed to function properly.
5	**Processor Error** - The CPU chip has generated an error.
6	**8042-Gate A20 Failure** - The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error message means that the BlOS is not able to switch the CPU into protected mode.
7	**Processor Exception lnterrupt Error** - The CPU chip has generated an exception interrupt.
8	**Display Memory Read /Write Error** - The video adapter is either missing or the video memory is faulty. PLEASE NOTE: This is not a fatal error.
9	**ROM Checksum Error** - The ROM checksum value does not match the value encoded in the BIOS.
10	**CMOS Shutdown Register Read/Write Error** - The shutdown register for the CMOS memory has failed.
11	**Cache Memory Read/Write Error** - A Cache Memory failure occurred, do not enable the Cache Memory to resume operation..