User's Manual
for the
IRV-686 Single Board Computer with VGA

MCSI PART NO. 88200 IRV-686
All-In-One Single Board Computers
For Industrial/Embedded Systems Applications

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Revised April 6, 1999
Revision 1.3

Changes are made periodically to the information contained herein; these changes will be incorporated into new editions of this document.

Requests for copies of this publication or the product(s) which it describes should be made to MCSI.

PREFACE

This manual provides information about the MCSI IRV-686 All-In-One Single Board Computer. This information is intended for users who must implement IBM PC/AT compatible computer solutions to a wide variety of applications which cannot be satisfied using conventional desktop computers. This manual assumes that the reader has a good understanding of MS-DOS and the standard IBM PC/AT compatible architecture. For more information on the IBM PC compatible hardware and software architecture, refer to any of the many books available on the subject. A few suggestions are listed below:

- *Advanced MS-DOS Programming*, Microsoft Press
- *Programmers Guide to the IBM PC*, Microsoft Press
- *Programming the 80386*, Sybex
- *Undocumented DOS*, Addison Wesley

INVENTORY CHECKLIST

The complete IRV-686 All-In-One Single Board Computer package consists of the following:

IRV-686 All-In-One Single Board Computer
PROMDISK-Chip Software Utilities with ROM-DOS ver 6.22 (optional)
VGA and E^2Key Software Utilities
This Manual

If any of the above is missing or appears to be damaged, inform MCSI immediately.

Table of Contents

SECTION 1 - INTRODUCTION

The MCSI IRV-686 Pentium/MMX All-In-One Single Board Computer (SBC) contains all the basic elements found in a high-performance IBM PC/AT compatible desktop computer system plus some unique features which make it ideally suited for industrial applications. The most outstanding features include: An optional 32MB PROMDISK-Chip™ Disk Emulator, dual PCI EIDE hard disk ports to support 4 EIDE drives, a high performance multi-I/O controller, a WatchDog timer, a 1K-bit E^2Key memory for user data, and user application addresses in the BIOS extension region of C800-EFFF. The board uses the Intel 430TX PCI Chipset which is PCI 2.1 compliant, and the S3 Virge/DX 3D VGA controller. The multi-I/O controller includes: dual 16C550 UARTs, a floppy port, and a SPP/EPP/ECP multi-mode bi-directional parallel port. The optional PROMDISK-Chip Disk Emulator comes complete with ROM-DOS version 6.22, making it ideal for embedded diskless applications. The 1K-bit E^2Key memory is a non-volatile memory is useful for storing user data, such as: critical system parameters, terminal address, etc. The WatchDog timer is ideal for controlling critical processes where unattended operation is essential.

The IRV-686 SBC is fully compatible with the IBM PC/AT ISA Bus and the PCI Bus version 2.1 which means virtually all the software written for the IBM PC/AT will run on the IRV-686 SBC.

FEATURES

A complete list of features is listed below:

- IBM PC/AT Compatible Plug-in Computer
- Supports 233MHz Pentium/MMX, AMD K6-2 and Cyrix 6x86 type CPUs up to 333MHz
- Includes Zero Insertion CPU Socket
- Intel 430TX Chip Set
- AWARD Plug-n-Play Flash BIOS
- Passive Backplane Architecture
- Includes 32 bit PCI 2.1 Compatible Bus
- S3 Virge/DX 3D VGA Controller and 2MB EDO Video Ram
- 256M-Byte High Performance SDRAM System Memory (2-168 pin DIMMs)
- 512KB Pipelined Burst Mode Secondary Cache
- Dual Floppy Disk Port Supports Two 3.5" or 5.25" Drives up to 2.88M-bytes
- PCI Extended EIDE Hard Disk Port supports up to Four Drives
- PS2/AT Compatible Keyboard Port
- PROMDISK-Chip Socket Supports up to 32MB PROMDISK-Chip Disk Emulator
- PS2 Compatible Mouse Port
- Two High Speed 16C550 Compatible RS-232 Serial Ports
- Multimode Bi-directional Parallel Printer Port
- Dual Universal Serial Bus Ports for future expansion
- Infrared Data Access Port for future applications
- Clock/Calendar with Battery Back-up
- Low Power CMOS Design
- Full Size AT Plug-in Multilayer Board for Low EMI and High Reliability
- WatchDog Timer and Power Monitor
- On-board Mini Speaker
- Optional External Reset
- Optional *Datalight* ROM-DOS 6.22 Operating System

SECTION 2 - SYSTEM DESCRIPTION

The following sections describe the major system features of the IRV-686 All-In-One Single Board Computer.

PROCESSOR

The IRV-686 Pentium SBC supports 100MHz to 233MHz Pentium/MMX, and the AMD K6-2 processor up to 333MHz. It also supports the Cyrix 6x86-PR266. The Pentium microprocessor includes an on-chip 16K-byte unified instruction cache, an 16K-byte data cache, an internal high performance math co-processor, and an enhanced 64-bit data bus. The on-board jumper selectable clock generator and ZIF CPU socket makes upgrading to a higher performance CPU easy. Some of the distinctive features of the processors include:

- 64-bit External Data Bus
- 32-bit Internal Architecture
- 256M-byte Directly Addressable Memory Space
- Internal 14 Word by 32-bit Register Set
- Separate 8K-byte Data and Cache Memories
- On-chip Pipelined Floating Point Processor
- Integrated Memory Manager

SYSTEM MEMORY (DRAM)

The IRV-686 Pentium SBC can support up to 256M-bytes of synchronous dynamic random access memory (SDRAM) organized as two banks of 16Mx72 including eight parity bits. The memory is configured using two dual in-line memory module sockets, which will accept 168-pin dual in-line memory modules (DIMMs) organized as 16MB, 32MB, 64MB, or 128MB with a maximum access time of 15ns.

CACHE MEMORY

The IRV-686 SBC includes 512K-bytes of pipelined burst mode cache memory for high speed access to blocks of data most recently read from main memory, including buffered data from the disk and video memory. The cache memory will significantly increase system performance over that of a conventional non-cached system.

DMA CONTROLLER

The IRV-686 SBC memory refresh and DMA functions are included in the System Controller chip which includes the equivalence of two 82C37 DMA controllers. The two DMA controllers are cascaded to provide four DMA channels for transfers to 8-bit peripherals (DMA1) and three channels for transfers to 16-bit peripherals (DMA2). DMA2 Channel 0 provides the cascade interconnection for the two DMA devices thereby maintaining IBM PC/AT compatibility. The DMA channel assignments are listed below:

DMA Channel 0: Not Used (8-bit)
DMA Channel 1: Alternate for Multi-mode Parallel Port (8-bit)
DMA Channel 2: Floppy Disk (8-bit)
DMA Channel 3: Multi-mode Parallel Port (8-bit)
DMA Channel 5: Not Used (16-bit)
DMA Channel 6: Not Used (16-bit)
DMA Channel 7: Not Used (16-bit)

The DMA request (DRQx) and acknowledge (DACKx/) lines are available on the P1 98-pin edge connector.

INTERRUPT CONTROLLER

The IRV-686 SBC has the equivalence of two 82C59A interrupt controllers included in the System Controller chip. The controllers accept requests from peripherals, resolve priorities on pending interrupts and interrupts in service, interrupt the CPU, and provide the vector address of the interrupt service routine. The two interrupt controllers are cascaded in a fashion compatible with the IBM PC/AT. The interrupt priority and assignments are shown below in descending order of priority:

Highest	IOCHCK/	Parity Check (Non-maskable)
	IRQ0	System Timer (Not Available)
	IRQ1	Keyboard (Not Available)
	IRQ8	Real Time Clock (Not Available)
	IRQ9	SVGA Controller
	IRQ10	Not Used
	IRQ11	Not Used
	IRQ12	Not Used
	IRQ13	Co-processor (Not Available)
	IRQ14	EIDE Disk Controller
	IRQ15	Not Used
	IRQ3	Serial Port 2
	IRQ4	Serial Port 1
	IRQ5	Alternate for Parallel Port
	IRQ6	Floppy Disk Controller
Lowest	IRQ7	Parallel Port

The interrupt request lines IRQx and IOCHCK/ are available on the 98-pin edge connector except as noted above.

TIMERS

The IRV-686 SBC has the equivalence of an 82C54 Programmable Timer included in the System Controller chip. The 82C54 is a three channel Programmable Counter/Timer chip. The three timers are driven by a 1.19MHz clock source derived from the on-board 14.31818MHz crystal oscillator. The three timers are used as follows:

TIMER Channel 0: System Timer
TIMER Channel 1: Timer for DRAM refresh
TIMER Channel 2: Tone Generation for Audio

CLOCK/CALENDAR AND CMOS RAM

The IRV-686 SBC includes an MC146818 compatible real time clock/calendar with 128 bytes of CMOS RAM. An on-board industrial Lithium battery (-40° to 85°, @ 850mAH) which provides over 10 years of data retention when the system power is off.

The 128 byte CMOS RAM consists of 14 bytes used by the clock/calendar, and 114 bytes used by the system BIOS.

Should your CMOS become corrupted, i.e. loss of battery power or accidentally clobbered, strange errors may occur while attempting to run your programs. Jumper JP1 is provided to clear the CMOS memory, refer to Section 3.0 for instructions on resetting the initial SETUP values. Refer to Appendix E for the jumper location.

KEYBOARD PORT

The IRV-686 SBC contains an IBM PC/AT compatible keyboard controller for interfacing to a generic IBM PC/AT compatible keyboard. The keyboard controller assembles the serial data from the keyboard into bytes and interrupts the CPU via IRQ1 after each byte is ready to be read. The IRQ1 service routine reads port 60H to get the keyboard scan code and acknowledges by sending a positive pulse to port 61H to clear the interrupt for the next byte. Refer to Appendix D for the keyboard connector location and pin assignments.

MOUSE PORT

The IRV-686 SBC contains an IBM PS2 compatible mouse port for interfacing to a generic serial mouse. The mouse port controller assembles the serial data from the mouse into bytes and interrupts the CPU via IRQ1 after each byte is ready to be read. The IRQ1 service routine reads port 60H to get the scan code and acknowledges by sending a positive pulse to port 61H to clear the interrupt for the next byte. Refer to Appendix D for the mouse port connector location and pin assignments.

SPEAKER PORT

The IRV-686 SBC contains an on-board sub-miniature audio speaker to provide audio interface to the user. Because of the small size of the speaker, the sound output is much reduced over that of the larger speaker found in most desktop computers. A connector is provided to connect an external speaker if the sound output is not sufficient. Refer to Appendix D for the speaker port connector location and pin assignments.

RESET SWITCH

The IRV-686 SBC includes an on-board power detector and power on reset circuit to reset the computer after power is applied, and to hold the computer reset during low power, brown-out

conditions. In addition, there are provisions for connecting an external, normally open, push button reset switch. Refer to Appendix D for the reset switch connector location and pin assignments.

PRINTER PORT

The IRV-686 SBC contains a multimode parallel port which has the equivalence of an IBM PC/AT Parallel Printer Port. The multimode parallel printer port supports the PS/2 type bi-directional parallel port (SPP), the enhanced parallel port (EPP), and the extended capabilities port (ECP) parallel port modes. The port can be configured as a standard IBM PC/AT compatible LPT1, LPT2, or LPT3 printer port, or disabled completely using the CMOS Setup utility. Refer to Appendix D for the connector location and pin assignments.

SERIAL PORTS

The IRV-686 SBC has the equivalence of two NC16C550 UARTs. The two UARTs can be configured as standard IBM PC/AT RS-232C compatible COM1, COM2, COM3, or COM4 serial ports or individually disabled using the CMOS Setup utility. The data rates are independently programmable up to 115.2K baud. Refer to Appendix D for the connector location and pin assignments.

FLOPPY DISK PORT

The IRV-686 SBC contains an IBM PC/AT compatible dual floppy disk port with the equivalence of an NEC PD72056B Floppy Disk Controller, an on-chip digital data separator, and an IBM PC/AT compatible floppy disk adapter bus interface circuit. The Floppy Disk Port can be disabled by using the CMOS Setup utility. An on-chip digital data separator provides optimum performance with the following disk drive types:

5.25"	360K Double-Sided
3.5"	720K High Capacity
5.25"	1.2M High Capacity
3.5"	1.44M High Density
3.5"	2.88M High Density

Refer to Appendix D for the connector location and pin assignments.

IDE HARD DISK PORT

The IRV-686 SBC contains two PCI Extended Integrated Drive Electronics (EIDE) Ports which directly interfaces to up to four hard disk drives with embedded controllers. The EIDE Disk Port can be disabled using the CMOS Setup utility. Refer to Appendix D for the connector location and pin assignments.

VGA DISPLAY PORT

The IRV-686 SBC includes a S3 Virge/DX 3D VGA display controller which interfaces directly to the local on-board PCI bus. The VGA display port is fully compatible with IBM VGA, EGA, CGA, and MDA display adapters, and provides improved performance and additional functionality. The S3 Virge/DX 64-bit DRAM-based accelerator combines a 135MHz RAMDAC and clock synthesizer with the multimedia capabilities including video acceleration, video playback using both software and hardware sources, live video support and the ability to connect with popular NTSC and PAL decoders. Additionally, S3 Virge/DX is SVGA-compatible, so as to support legacy DOS applications and games, and provides high-performance 2D GUI acceleration support for resolutions up to 1280 x 1024 x 256 colors at 75Hz. It also provides support for all major 3D APIs, including OpenGL, Microsoft's Direct3D and RealityLab, as well as Argonaut BRender and Criterion Renderware. The board includes 2M-bytes of high speed EDO DRAM. Drivers and programming information can be obtained directly from S3's Website http://www.s3.com. Refer to Appendix D for connector location and pin assignments.

WATCHDOG TIMER

The IRV-686 SBC includes a WatchDog Timer circuit. The WatchDog Timer ensures that if an application program gets "lost or bombs", the system will reset or a non-maskable interrupt will be issued to the CPU. The WatchDog Timer is enabled by reading I/O port 443H. Once enabled, the WatchDog Timer must be triggered by reading I/O port 443H within the time out period, otherwise the WatchDog Timer will force a hardware reset or activate the IOCHCK/ line, generating a non-maskable interrupt (NMI). The WatchDog Timer can be disabled by reading I/O port 43H. A jumper is provided to select the time out period and to enable the WatchDog Timer circuit. Refer to Appendix E for the WatchDog Timer configuration jumpers.

OPTIONAL PROMDISK-CHIP DISK EMULATOR

The IRV-686 includes a socket designed to accept the MCSI PROMDISK-Chip. The PROMDISK-Chip Disk Emulator is a unique Flash Memory array which emulates a bootable read/write hard disk drive. The PROMDISK-Chip is offered in 4M, 8M, 16M, and 32M byte capacities and comes complete with ROM-DOS version 6.22 installed. The PROMDISK-Chip occupies an 8K block of memory space above 640K, whose starting address is selected by jumper JP9. The PROMDISK-Chip uses the Datalight Flash/FX integrated Flash File System and boot utilities. Refer to Appendix E for the jumper location.

The Flash/FX Variable Block Flash (VBF) File System and ROM-DOS allow the PROMDISK-Chip to operate as a non-volatile Read/Write disk drive. This means that you can list directories, copy files, and read and write to the Flash memory on PROMDISK-Chip through standard DOS interrupts and commands.

HIGH SPEED PCI EXPANSION BUS

The IRV-686 SBC is equipped with a high speed PCI expansion bus which allows the use of high speed I/O controllers such as SVGA, SCSI, Ethernet Network, and Serial Communications adapters. The PCI expansion bus is compatible with the PICMG (PCI Industrial Computer Manufacturers Group) 2.1 standard and supports up to 4 PCI master peripheral boards.

UNIVERSAL SERIAL BUS PORT

The IRV-686 SBC contains two Universal Serial Bus Ports for the future I/O expansion bus. Refer to Appendix D for connector location and pin assignments.

IrDA Infrared Interface Port

The IRV-686 SBC contains a built in IrDA infrared interface port which supports Serial Infrared (SIR) or Amplitude Shift Keyed IR (ASKIR) interfaces. The IrDA port is addressed as COM2 and must be setup in the BIOS' Peripheral Setup. When the IrDA port is enabled, the standard COM2 serial port is disabled. Refer to Appendix D for connector location and pin assignments.

Flash EPROM BIOS

The IRV-686 SBC contains a 128KB Flash EPROM which contains the Award Plug-n-Play system BIOS. The Flash EPROM can be programmed on-board with the programming software utility when a new udated version of the BIOS is released.

E^2 Key 1K-bit User EEPROM

The IRV-686 SBC includes the E^2 Key 1K-bit electrically eraseable memory. This memory is useful for storing user data such as password, terminal address, configuration parameters, etc. The memory is configured as 64 words, which can be accessed a word at a time, and uses the parallel port for the hardware interface. Software utilities are provided on the distribution disk which includes a demo program, and two C library functions for integrating into your application program.

Cooling Fan Control

The IRV-686 SBC provides connectors for the CPU and chassis cooling fans. These connectors provide +12VDC at 500ma and a "Fan Rotation" signal input. The fan rotation signal is used by the system BIOS power management feature. Refer to Appendix D for connector location and pin assignments.

ATX Power Supply Features

The IRV-686 SBC provides interface connectors to support ATX power supplies. When using an ATX power supply, you must connect the +5V "Standby" signal on connector JP3 pins 18 & 20 to +5VDC on the power supply to enable the standby feature. Connector JP3 pin 17 is used interface to ATX power supplies that use a momentary switch to control the ON/SLEEP (OFF) function. Pushing the switch once will toggle between the ON and SLEEP modes; pushing the switch for more than four seconds will turn the system power off. Refer to Appendix D for connector location and pin assignments.

SECTION 3 - SETUP

The IRV-686 SBC uses the latest AWARD Plug-n-Play BIOS which contains an internal Setup Utility for configuring the system. The BIOS includes a graphical user interface, and a new system configuration utility, as well as all the features of the standard BIOS. The system configuration settings are stored in the on-board CMOS memory which is backed up by a Lithium battery. Should your CMOS become corrupted, i.e. loss of battery power or accidentally clobbered, strange errors may occur while attempting to run your programs. A jumper at JP1 has been provided to force the BIOS to use its internal default SETUP values. This is accomplished by first removing power from the IRV-686 and momentarily interrupting the battery power to the system controller chip. To interrupt the battery power, remove the shunt from pins 1 & 2 and momentarily connect it to pins 2 & 3 (the "Clear CMOS" position). After waiting a few seconds, return the shunt back to its original position. Refer to Appendix E for the jumper location.

WARNING: DO NOT apply power to the IRV-686 with the shunt in the clear CMOS position -- serious damage will result.

The Setup Utility can be invoked by first causing a cold boot (reset) or a warm boot (**Cntrl Alt Del)** and pressing the **Del** key when instructed. This will cause the memory diagnostics to be aborted and the Setup Utility to display the MAIN SETUP MENU. Using the →↑↓← cursor keys, move the highlighted bar to the option you wish to modify and then press **Enter** to select it. When in the MAIN SETUP MENU, the **F2** key is used to select the colors used in the setup screens, and the **F10** key is used to save the changes before exiting the Setup Utility. The **Esc** key may be used to exit the Setup Utility without saving the changes. The **PgUp** and **PgDn** keys are used to scroll through the selections for a given setting. **PgUp** is also used to decrease the setting and **PgDn** to increase the setting. In addition, you may also enter the setup utility directly by pressing the **Cntrl Alt Esc** simultaneously.

After making the desired selections from the various setup menus, you can save your selections by pressing the **F10** key or by selecting the appropriate selection from the MAIN SETUP MENU.

Notes:

1. The user should be aware that improper selection of certain values in the CHIPSET, POWER MANAGEMENT, and PNP/PCI selections may cause unpredictable results. If this occurs select the LOAD BIOS DEFAULTS from the MAIN SETUP MENU and then press the **F10** to save and exit.

SECTION 4 - USING THE PROMDISK-CHIP DISK EMULATOR

The IRV-686 SBC includes a 32-pin socket which supports the MCSI PROMDISK-Chip disk emulator which operates as a Read / Write fixed disk drive. The paragraphs that follow describe how to use the optional PROMDISK-Chip.

USING ROM-DOS AND OTHER DISK OPERATING SYSTEMS

The PROMDISK-Chip has been preconfigured at the factory with the latest version of the Datalight ROM-DOS disk operating system. In addition, a current copy of the operating system is supplied on a floppy diskette.

If the operating system is accidentally erased from the PROMDISK-Chip it may be restored using the SYS command. The DOS format utility should not be used to restore the operating system.

To change the operating system version or type you should simply use the equivalent DOS SYS command to transfer the operating system.

PROMDISK LOW LEVEL FORMAT

The Flash memory contained on the PROMDISK-Chip board was initialized with the Datalight CardTrick low level format at the factory. During normal operation the Flash memory should never require reformatting unless there is a serious hardware or software malfunction. In the event it has been determined that the low level format is corrupted, proceed as follows:

1. At the DOS prompt, run the PROMDISK-Chip low level format utility PDCFMT.EXE located on the distribution diskette in the PDCHIP3 subdirectory.
2. Install a bootable floppy diskette in drive A and boot the system.
3. At the DOS prompt type SYS C: to transfer a bootable copy of DOS to PROMDISK-Chip.
4. Remove the floppy diskette from drive A: and reboot the system from PROMDISK-Chip.

CAUTION: Do Not use the DOS Fdisk utilities on the PROMDISK-Chip.

SECTION 5 - INSTALLATION

This section describes the procedures for installing the IRV-686 All-In-One Single Board Computer into your system. The following is a list of typical peripherals required to build a minimum system:

- Passive Backplane and Power Supply
- IBM PC / AT Type Keyboard
- Display Adapter and Monitor
- Floppy or Hard Disk with MS-DOS, ROM-DOS, or PROMDISK Disk Emulator

INSTALLING THE DIMMS

When installing or removing the DRAM DIMMs, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the DIMMs:

1. Insert the first DIMM edge connector into the DIMM1 socket closest to the top of the board. Note that the DIMMs are keyed and will only go in one way.

2. Push the DIMM into the connector carefully until it snaps into place.

3. Check to make sure the DIMM is inserted securely.

4. Insert the second DIMM edge connector (if required) into the DIMM2 socket.

To remove a DIMM, move the locking ejector tabs outward on each side of the DIMM and lift the DIMM from the connector.

INSTALLING THE CPU

When installing or removing the CPU, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the CPU:

1. Open the ZIF socket by lifting the release arm to its vertical position causing the sliding base plate to move to the open position.

2. Align pin one (white dot or beveled edge) on the CPU chip with pin one of the ZIF (zero insertion force) socket. Note pin 1 of the ZIF socket is located on the bottom left side of the socket. To complete the installation gently press the CPU chip into place and return the release arm to its locked position.

3. Double check the insertion and orientation of the chip before applying power. Improper installation will result in permanent damage to the chip. Refer to Appendix E for CPU speed and configuration jumpers.

To remove the CPU chip, open the ZIF socket by lifting the release arm to its vertical position and gently remove the chip.

INSTALLING THE PROMDISK-CHIP

When installing or removing the PROMDISK-Chip, be sure to first touch a grounded surface to discharge any static electricity from your body. Use the following procedure to install the PROMDISK-Chip:

1. Align pin one (square pad) on the PROMDISK-Chip with pin one of socket U11 on the CPU board.

2. Push the PROMDISK-Chip into the socket carefully until it is fully seated.

3. Check to make sure the PROMDISK-Chip is installed securely, and there are no bent pins.

To remove the PROMDISK-Chip, insert a small screwdriver between the PROMDISK-Chip and the socket and gently pry around the edge until the PROMDISK-Chip is released from the socket.

COMPLETING THE INSTALLATION

To complete the installation, the following steps should be followed:

1. Set the configuration jumpers in accordance with Appendix E.

2. Install the IRV-686 SBC into one of the I/O slots in a passive backplane.

3. Connect the applicable I/O cables and peripherals, i.e. floppy disk, IDE hard disk, monitor, keyboard, power supply, etc.

4. Connect an IBM PC compatible keyboard.

5. Turn power on to the display monitor.

6. Turn power on to the backplane power supply.

7. After the BIOS sign-on message is displayed, press the **Del** key to enter the Setup Utility.

8. Reconfigure the IRV-686 CMOS using the internal SETUP.

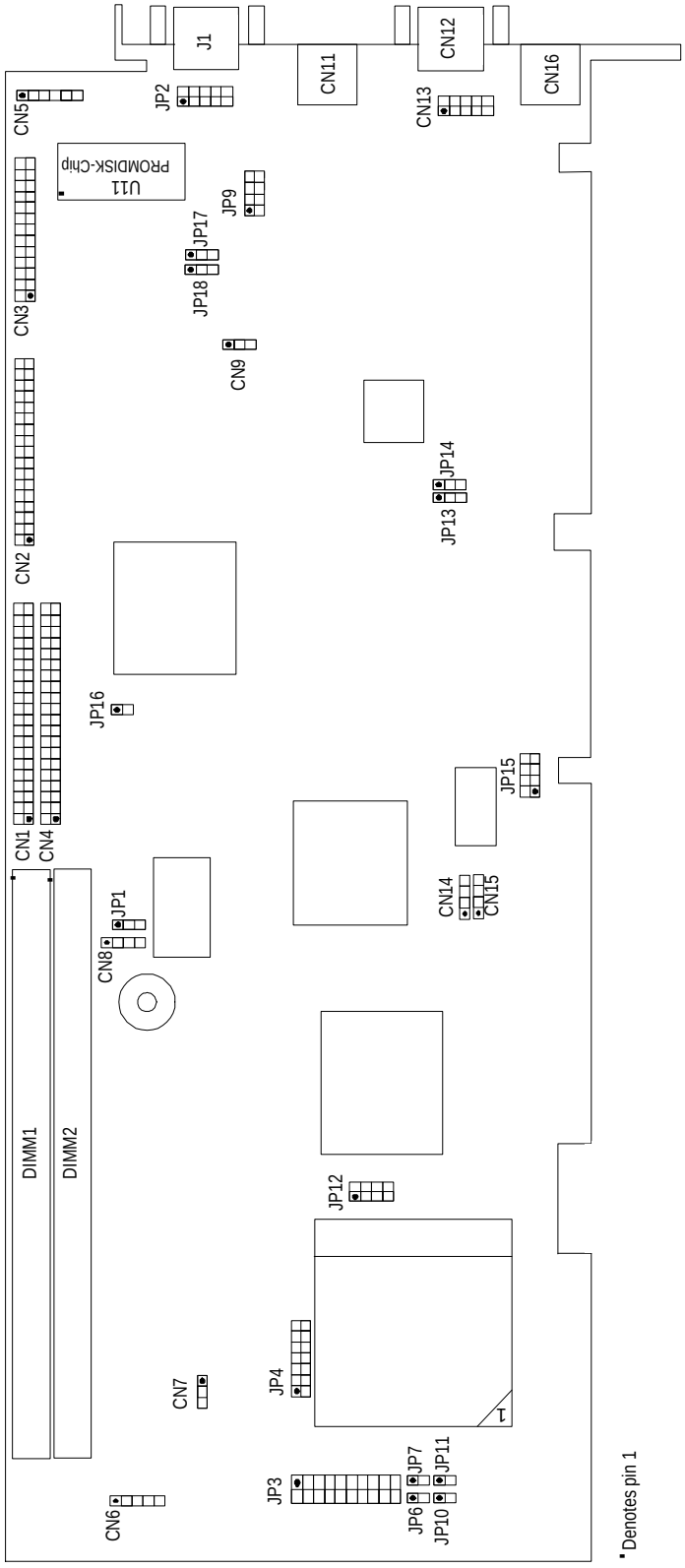
9. Boot the system.

APPENDIX A - SPECIFICATIONS

This appendix lists the specifications for the IRV-686 All-In-One Single Board Computer.

CPU:	Supports: Intel Pentium/MMX up to 233MHz, AMD K6-2 up to 333MHz, and Cyrix 6x86 processors up to 266MHz.
Co-processor:	Internal to the Pentium Chip
Memory:	System Memory Expandable to 256M-bytes. Supports: 8MB, 16MB, 32MB, 64MB, or 128MB SDRAM DIMMs using two 168-pin DIMM sockets. Internal 16K-byte Data and 16K-byte Instruction Cache Memory. 512K-bytes of High Speed pipelined burst mode Cache Memory.
BIOS:	AWARD Plug-n-Play BIOS Flash EPROM.
Clock/Cal:	PC/AT Compatible with on-board Lithium battery back-up
I/O Bus:	IBM PC/AT Compatible 98-pin Edge Connector
PCI Bus:	Industry Standard version 2.1 PICMG high performance I/O bus.
DMA:	7 Channels (4 8-bit & 3 16-bit) PCI Ultra DMA/33
Timers:	3 Programmable
Interrupts:	16
Reset:	Controlled by on-board power detector with provisions for external reset switch at header JP3
I/O Ports:	2 - RS-232 Serial Ports (CN12 at rear connector, and CN13 header) 1 - Parallel Printer Port (at connector CN3) 1 - PS2 Keyboard Port (at header CN6 and at rear PS2 type connector CN16) 1 - On-board Speaker with Speaker Port (JP3) 1 - Dual 3.5"/5.25" Floppy Disk Port (CN2) 2 - IDE Hard Disk Port (Primary at CN1 & Secondary at CN4) 1 - WatchDog Timer 1 - PS2 Mouse Port (CN11) 1 - IDE LED Port (JP3) 1 - Keylock & Power LED (JP3) 2 - Universal Serial Bus Ports (at headers CN14 and CN15) 1 - IrDA Infrared Port (CN5)
PCI Video Port:	1 - PCI VGA Video Port (at rear connector J1 and header JP2) Chipset: S3 Virge/DX 3D Video Controller VRAM: 2MB EDO DRAM Resolution: 1280 x 1024, 256 color,75Hz 1024 x 768, 64K color, 75Hz 800 x 600, full color, 90Hz
Speed:	100-333MHz jumper selectable.
Battery:	Lithium for Clock/Calendar & CMOS RAM (ten years typical)
Benchmark:	LANDMARK v2.0 =1344MHz for 233MHz 6x86
Size:	Full Size AT board 13.3"L X 4.8"H
Weight:	12 Oz.
Power:	+5VDC @ 4.8A, ±12VDC @ 0.070A

APPENDIX B - BOARD OUTLINE



APPENDIX C - MEMORY AND I/O MAPS

The following is the memory map for the IRV-686 SBC. The addresses are fully PC/AT compatible, unless otherwise specified.

IRV-686 SBC Memory Map

Address	Used For	Size
00000H - 003FFH	Interrupt Vectors	1.0K
00400H - 005FFH	BIOS Values	0.5K
00600H - 9FFFFH	User RAM (DOS)	638.5K
A0000H - AFFFFH	Reserved for VGA	64.0K
B0000H - B7FFFH	Video RAM (MDA)*	32.0K
B8000H - BFFFFH	Video RAM (CGA)*	32.0K
C0000H - C3FFFH	Reserved	16.0K
C4000H - C7FFFH	EMS Window	16.0K
C8000H - DFFFFH	ROM Scan Devices*	96.0K
E0000H - FFFFFH	System BIOS	128.0K
100000H - FFFFFFFH	User Memory	256.0M

External to the IRV-686

The following is the I/O map for the IRV-686 SBC. I/O addresses are fully PC/AT compatible, unless otherwise specified.

IRV-686 SBC I/O Map

Address	Function
000H - 01FH	DMA Controller #1
020H - 021H	Interrupt Controller #1
022H - 023H	Configuration Address Register
040H - 05FH	System Timers & WatchDog Timer
060H - 063H	Keyboard, Status, & System Control
070H - 07FH	Clock/Calendar & CMOS Ram Access
080H - 083H	DMA Page Register
0A0H - 0BFH	Interrupt Controller #2
0C0H - 0DFH	DMA Controller #2
0F0H	Clear Math Co-processor Busy
0F1H	Reset Math Co-processor
1F0H - 1F8H	IDE Hard Disk
278H - 27FH	Parallel Printer Port LPT2
2E8H - 2EFH	Serial Port COM4
2F8H - 2FFH	Serial Port COM2
378H - 37FH	Parallel Printer Port LPT1
3BCH - 3BFH	Parallel Printer Port LPT3
3E8H - 3EFH	Serial Port COM3
3F0H - 3F7H	Floppy Disk Controller
3F8H - 3FFH	Serial Port COM1
043H	Disable WatchDog Timer
443H	Enable WatchDog Timer

APPENDIX D - CONNECTORS

CN6 Keyboard Header/Connector

Pin	Signal
1	KBCLK
2	KBDATA
3	N/C
4	GND
5	+5VDC

CN16 Keyboard Connector (PS2 type)

Pin	Signal
1	KBDATA
2	N/C
3	GND
4	+5VDC
5	KBCLOCK
6	N/C

JP3 Keylock Header/Connector

Pin	Signal Name	Description
2	LED POWER (+)	Connect to anode of power LED
4	N/C (Key)	N/C (Key)
6	GND	Connect to cathode of power LED
8	KB LOCK/	Connect to ground to inhibit keyboard
10	GND	Ground

CN2 Floppy Disk Port Connector

Pin	Signal Name
2	RPMLC
4	Not Used
6	Not Used
8	INDEX/
10	MOTOR0/
12	DRIVE SELECT1/
14	DRIVE SELECT0/
16	MOTOR1/
18	DIRECTION
20	STEP/
22	WRITE DATA/
24	WRITE GATE/
26	TRACK0/
28	WRITE PROTECT/
30	READ DATA/
32	HEAD SELECT/
34	DISK CHANGE/

All odd numbered pins are GND

CN1 & CN4 IDE Hard Disk Port Connectors

Pin	Signal	Pin	Signal
1	IDERST/	2	GND
3	IDED7	4	IDED8
5	IDED6	6	IDED9
7	IDED5	8	IDED10
9	IDED4	10	IDED11
11	IDED3	12	IDED12
13	IDED2	14	IDED13
15	IDED1	16	IDED14
17	IDED0	18	IDED15
19	GND	20	Not Used
21	Not Used	22	GND
23	IDEIOW/	24	GND
25	IDEIOR/	26	GND
27	Not Used	28	IDEALE
29	Not Used	30	GND
31	IRQ14	32	IOCS16/
33	IDESA1	34	Not Used
35	IDESA0	36	IDESA2
37	HDCS0/	38	HDCS1/
39	IDEACT/	40	GND

CN3 Printer Interface Connector

Pin	Signal	Pin	Signal
1	STROBE/	14	AUTOFD/
2	PDAT0	15	ERROR/
3	PDAT1	16	INIT/
4	PDAT2	17	SLCTIN/
5	PDAT3	18	GND
6	PDAT4	19	GND
7	PDAT5	20	GND
8	PDAT6	21	GND
9	PDAT7	22	GND
10	ACK/	23	GND
11	BUSY	24	GND
12	PE	25	GND
13	SLCT	26	GND

CN12 Serial Port #1 9-pin Sub D Connector

Pin	Signal Name
1	CARRIER DETECT #1
2	RECEIVE DATA #1
3	TRANSMIT DATA #1
4	DATA TERMINAL READY #1
5	GND
6	DATA SET READY #1
7	REQUEST TO SEND #1
8	CLEAR TO SEND #1
9	RING INDICATOR #1

CN13 Serial Port #2 10-pin Header/Connector

Pin	Signal Name
1	CARRIER DETECT #2
2	DATA SET READY #2
3	RECEIVE DATA #2
4	REQUEST TO SEND #2
5	TRANSMIT DATA #2
6	CLEAR TO SEND #2
7	DATA TERMINAL READY #2
8	RING INDICATOR #2
9	GND
10	N/C

J1 VGA Display Connector (15-pin Sub-D)

Pin	Signal	Pin	Signal
1	RED	2	GREEN
3	BLUE	4	N/C
5	GND	6	GND
7	GND	8	GND
9	N/C	10	GND
11	N/C	12	N/C
13	HSYNC	14	VSYNC
15	N/C		

JP2 VGA Display Header

Pin	Signal	Pin	Signal
1	RED	2	GND
3	BLUE	4	GND
5	GREEN	6	GND
7	HSYNC	8	GND
9	VSYNC	10	GND

JP3 Speaker Port Header/Connector

Pin	Signal Name	Description
1	SPEAKER	Connect to Speaker (-)
3	N/C	No Connection
5	N/C	No Connection
7	+5VDC	Connect to Speaker (+)

JP3 Reset Header/Connector

Pin	Signal Name	Description
9	RESET/	Connect to switch, ground this pin to reset
11	GND	Ground

JP3 IDE LED Header/Connector

Pin	Signal Name	Description
13	IDE LED	Connect to IDE LED anode (-)
15	+5VDC	Connect to IDE LED cathode (+)

CN11 PS2 Mouse Connector

Pin	Signal
1	MSDATA
2	N/C
3	GND
4	+5VDC
5	MSCLK
6	N/C

CN14 & CN15 Universal Serial Bus Ports 1 & 2 Connectors

Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

CN5 IrDA Infrared Port Connector

Pin	Signal
1	+5VDC
2	FIR-RX
3	IR-RX
4	GND
5	IR-TX
6	CIRRX

CN8 External Battery Connector

Pin	Signal
1	EXT +
2	N/C
3	N/C
4	EXT -

Note: Remove jumper from 1-2 when using external battery.

CN7 CPU Fan Connector

Pin	Signal
1	Rotation Signal
2	+12V
3	GND

CN9 Chassis Fan Connector

Pin	Signal
1	Rotation Signal
2	+12V
3	GND

JP3 ATX Power Supply Power Switch Control

Pin	Signal
17	Switch (+)
19	Switch (-)

JP3 Standby Connector for ATX Power Supply

Pin	Signal

12	GND
14	No Connection
16	Suspend Control Signal
18	+5V Standby Signal
20	+5V Standby Signal

APPENDIX E - CONFIGURATION JUMPERS

JP4 CPU Clock Jumper

Frequency	1-2	3-4	11-12	13-14
55MHz	OFF	ON	ON	OFF
60MHz	OFF	ON	OFF	OFF
66MHz	OFF	OFF	OFF	OFF

JP4 CPU Clock Multiplier Jumper

Multiplier	5-6	7-8	9-10
1.5X	OFF	OFF	OFF
2X	ON	OFF	OFF
2.5X	ON	ON	OFF
3X	OFF	ON	OFF
3.5X	OFF	OFF	OFF
4X	ON	OFF	ON
4.5X	ON	ON	ON
5X	OFF	ON	ON
5.5X	OFF	OFF	ON

JP12 CPU Core Voltage Jumper

Voltage	1-2	3-4	5-6	7-8
3.5V	ON	ON	ON	ON
3.4V	OFF	ON	ON	ON
3.3V	ON	OFF	ON	ON
3.2V	OFF	OFF	ON	ON
3.1V	ON	ON	OFF	ON
3.0V	OFF	ON	OFF	ON
2.9V	ON	OFF	OFF	ON
2.8V	OFF	OFF	OFF	ON
2.7V	ON	ON	ON	OFF
2.6V	OFF	ON	ON	OFF
2.5V	ON	OFF	ON	OFF
2.4V	OFF	OFF	ON	OFF
2.3V	ON	ON	OFF	OFF
2.2V	OFF	ON	OFF	OFF
2.1V	ON	OFF	OFF	OFF
2.0V	OFF	OFF	OFF	OFF

JP10, JP11, JP6, & JP7 Dual/Single Voltage Select Jumpers

CPU	JP10	JP11	JP6	JP7
Pentium	ON	ON	OFF	OFF
Pentium/MMX AMD K5/K6-2 Cyrix 6x86 Dual Voltage	OFF	OFF	ON	ON

JP13 WatchDog Timer Control Jumper

2-3	Generates hardware RESET when time out occurs. (Default)
1-2	Generates NMI (IOCHRDY) when time out occurs.
OFF	Disable

JP15 WatchDog Timer Time-out Period Jumper

Time	1-2	3-4	5-6	7-8
1second	OFF	OFF	ON	OFF
2 seconds	OFF	OFF	ON	ON
10 (Default)	OFF	ON	OFF	OFF
20 seconds	OFF	ON	OFF	ON
110 seconds	ON	OFF	OFF	OFF
220 seconds	ON	OFF	OFF	ON

JP9 PROMDISK-Chip Address Jumper

Address	JP9
CE00H (C800H)	1-2
D600H (D000H)	3-4
DE00H (D800H)	5-6
Not Used	7-8

() Denotes PCB Rev 6.1 and earlier

JP1 Clear CMOS Setup Jumper

1-2	Normal Operation (Default)
2-3	Clear CMOS Setup

CN8 External Battery Connector

Battery	1-2	3-4
Internal	ON	OFF
External	OFF	OFF

JP14 BIOS Flash Chip Voltage Jumper

Voltage	JP14
5V Flash Voltage	2-3
12V Flash Voltage	1-2

JP16 PS/2 Mouse Interrupt Jumper

Interrupt	JP16
IRQ12	ON
Not Used	OFF

APPENDIX F - BIOS ERROR BEEP CODES

During the POST (Power On Self Test) routines, which are performed each time the system is powered on, errors may occur.

Nonfatal errors are those which, in most cases, allow the system to continue the boot up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with MCSI Customer Service for possible repairs.

These fatal errors are communicated through a series of audible beeps. The numbers on the fatal error list below correspond to the number of beeps for the corresponding error. All errors listed, with the exception of number eight, are fatal errors.

No. of Beeps	Error Message
1	**Refresh Failure** - The memory refresh circuitry is faulty.
2	**Parity Error** - A parity error was detected in the first 64K block of system memory.
3	**Base 64KB Memory Failure** - A memory failure occurred within the first 64KB of memory.
4	**Timer Not Operational** - Timer #1 has failed to function properly.
5	**Processor Error** - The CPU chip has generated an error.
6	**8042-Gate A20 Failure** - The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error message means that the BlOS is not able to switch the CPU into protected mode.
7	**Processor Exception lnterrupt Error** - The CPU chip has generated an exception interrupt.
8	**Display Memory Read /Write Error** - The video adapter is either missing or the video memory is faulty. PLEASE NOTE: This is not a fatal error.
9	**ROM Checksum Error** - The ROM checksum value does not match the value encoded in the BIOS.
10	**CMOS Shutdown Register Read/Write Error** - The shutdown register for the CMOS memory has failed.
11	**Cache Memory Read/Write Error** - A Cache Memory failure occurred, do not enable the Cache Memory to resume operation.